

Abstract

A power-saving clock divider scheme is cost-effective, flexible, jitterless, and allows the user to keep track of time. In general, the clock divider selectively operates in a normal mode and one or more divide modes, wherein the divide modes provide a clock frequency that is a fraction of the normal clock frequency by a divisor value that is specified in a user-accessible divider register. Lower divisor values (e.g., 2, 4, 8, etc.) are preferably used for performance tuning, while large divisor values (e.g., 1024, 2048, and 4096) are preferably used for power saving.